J. ALBERTO MORO

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PROFESSIONAL SUMMARY

Electronics and ICT Engineer specialized in Embedded systems and AI. With a passion for full-stack engineering from soldering prototypes to developing firmware and self-hosting a home-lab. Actively exploring hardware and software through custom electronics and digital signal processing projects.

EDUCATION

Master of Electronics and ICT Engineering Technology 2023 - 2025
University Of Antwerp (UA), Belgium

- Focused on modern engineering technologies, advanced ICT architectures, and AI integration.

Electronics Master Erasmus Program 2021
Linköping University (LiU), Sweden

- Specialized in IC analysis, hardware description languages and design and development using HDL (FPGAs).

Bachelors in Engineering Technologies and Telecommunication Services 2018 - 2023
Polytechnic University of Madrid (UPM), Spain

- Acquired a comprehensive theoretical and practical base across all critical fields of Telecommunications.

SKILLS

Hardware & Embedded	STM32, ESP32, FPGA (Verilog/VHDL), SPI/I2C/CAN, C/C++, Assembly
Edge AI & ML	TensorFlow Lite, PyTorch, Pruning and Quant., CNNs/RNNs, Edge Deployment
RF & Signal Processing	Beamforming, Antenna Arrays, DSP, SDR, Wave Propagation, Acoustics
Infrastructure & Systems	Linux Server, Docker, VMware ESXi, CUDA, CMake, Git/CI-CD
Languages	Spanish (Native), English (C1), Chinese (HSK2), Japanese (N4), Swedish (A1),French (A2)

EXPERIENCE

Firmware & Embedded Systems Intern 2023
INETUM (former Gfi group) *Madrid, Spain*

- Developed, debugged, and optimized firmware solutions for custom Linux-embedded hardware architectures.
- Enhanced system performance by programming and testing software layers interacting closely with hardware.
- Collaborated with cross-functional engineering teams to implement modern software development best practices.

PROJECTS

Embedded ML Sub-GHz RF Anomaly Detector. Developed a lightweight C++ inference pipeline utilizing spectral FFT analysis to detect real-time RF jamming attacks with over 94% validation accuracy. Optimized for Heltec ESP32-S3 boards running Meshtastic firmware, achieving a 1ms execution footprint using only 1.4KB RAM.

Real-Time BLE AoA Localization System. Engineered a low-latency 3D tracking platform using Silicon Labs BG22 dual-polarized antenna arrays and optimized MUSIC/Capon algorithms. Bypassed standard network layers via custom serial phase data streaming, hitting a 17.94ms end-to-end processing latency.

Parametric Jumping Round Robin Input Arbiter. Designed a scalable, generic network switch module in Verilog HDL to orchestrate multi-queue access to shared resources without idle clock cycles. Built a parallel combinational matrix layout targeted for Xilinx Virtex UltraScale+ FPGAs to achieve a 1-cycle switchover.